In the Specification:

On page 1, after the title insert the following:

RELATED APPLICATIONS

This is a U.S. national stage of application No. PCT/EP2005/002112, filed on February 28, 2005.

This patent application claims the priority of German patent application no. 10 2004 009 521.3 filed February 27, 2004, the disclosure content of which is hereby incorporated by reference.

FIELD OF THE INVENTION

On page 1, before line 11, insert the following heading:

BACKGROUND OF THE INVENTION

On page 2, after line 14, insert the following paragraphs:

EP 0 973 205 A2 describes a high-voltage MOS transistor with a drain extension in which the embedding n well has a lower depth underneath the drain extension than underneath the drain which is provided. The depth of the p-conductive well is greater in the area of the drain extension than underneath the drain which is provided. The points of least depth of the n well and greatest depth of the p well are offset with respect to one another.

Document R. Stengl and U. Gösele: "Variation of Lateral Doping - A New Concept to Avoid High Voltage Breakdown of Planar Junctions", International Electron Devices Meeting,

Technical Digest, 1 to 4 December 1985, pages 154 to 157 (XP002013050) describes a masking in order to manufacture a p-conductive well in which additional covers are provided in certain sections between the central area and the edge area of the well which is to be produced.

On page 2, before line 28, insert the following heading:

SUMMARY OF THE INVENTION

On page 2, amend the paragraph beginning on line 28 as follows:

~~The~~ One object of the invention is to ~~specify~~ provide an improved lateral high-voltage PMOS transistor, a mask or masking for the corresponding wells. ~~and~~ Another object of the invention is to provide a method for manufacturing the wells.

On page 2, delete the paragraph beginning on line 33 through line 35 in its entirety and insert the following:

These and other objects are attained in accordance with one aspect of the present invention directed to a high voltage PMOS transistor comprising an insulated gate electrode, a p-conductive source region in an n-conductive well which is arranged on a p-conductive substrate, a p-conductive drain region in a p-conductive well which is arranged in said n-conductive well, and an insulation area between said gate electrode and said drain region, wherein the depth of the n-conductive well underneath said drain region is less than underneath said source region, and the depth of the p-conductive well is greatest underneath the drain region.

Another aspect of the present invention is directed to a mask for manufacturing an n-conductive well of a high-voltage PMOS transistor, in which the area of the drain which is

provided is covered with a drain cover, and a further cover between the areas which are provided for the drain and the source is produced at a distance from the drain cover.

Another aspect of the present invention is directed to a masking for manufacturing a p-conductive well of a high-voltage PMOS transistor, in which additional covers are provided in certain sections between the central area and the edge area of the well which is to be produced, which widen in the direction from the source which is provided to the drain which is provided, and are spaced apart from one another.

Another aspect of the present invention is directed to a method for manufacturing an n-conductive well and a p-conductive well of a high-voltage PMOS transistor having a p-conductive drain region in the p-conductive well which is arranged in the n-conductive well, in which the implantation of ions is carried out by means of masks or maskings in such a way that the doping depth of the p-conductive well is greater under the drain which is provided than in the direction of the well areas which are assigned to the source.

On page 4, before line 15, insert the following heading:

BRIEF DESCRIPTION OF THE DRAWINGS

On page 4, after line 35, insert the following heading:

DETAILED DESCRIPTION OF THE DRAWINGS

On page 5, amend the paragraph beginning on line 13 as follows:

Field oxide areas 413 which have a window for reception of the highly doped, p-conductive drain 414 are provided in the direction of the drain. Underneath the drain 414 and the

field oxide areas 413, a p-doped well 412 is arranged within the n-doped well 411 which extends laterally into the channel zone K ~~area~~. The gate electrode 418 is lengthened in the direction of the drain 414 to cover an area of the field oxide 413. This area which lies above the p-doped well 412 serves as a field plate for controlling the electric field. The area of the p-doped well 412 between the drain 414 and the channel zone K serves as a drift area for the charge carriers, and in the lateral direction serves for reducing the electrical field.

On page 5, amend the paragraph beginning on line 27 through page 6, line 2 as follows:

In the exemplary embodiment, the high-voltage PMOS transistor is symmetrical with respect to the line L. In the vertical direction underneath the drain 414, points A", B" and C" are shown along the doped line L serving as a line of symmetry of the PMOS transistor. At the high potential which is present at the drain, the distance A"-B" must be dimensioned such that a punch through cannot occur between the p-doped well 412 and the substrate 410. At the same time, the distance A"-C" must be dimensioned such that the critical field strength occurring at the point A" is reduced if the drain contact 414 changes from a high voltage level to a low voltage level (substrate potential level).

On page 6, amend the paragraph beginning on line 30 through page 7, line 3 as follows:

In the exemplary embodiment in Figure 4, the p-n junction between the p-conductive substrate 410 and the n-doped well 411 is virtually flat. Likewise, the p-n junction between the p-doped well 412 and the n-doped well 411 underneath the drain 414 is very flat. The distance A"-C" is set by means of the diffusion step after the implantation. This distance is necessary since the spatial charge zone in the vicinity of the point A" must not extend as far as the p+

since the spatial charge zone in the vicinity of the point A" must not extend as far as the p+ diffusion region of the drain 414. At the same time, a predefined distance A"-B" is produced in order to prevent a punch through between the substrate and the p-doped well 412.

On page 7, amend the paragraph beginning on line 14 as follows:

The channel K and a p-doped well 12 are firstly adjacent ~~from~~ to the source region 15 in the direction of the highly doped, p-conductive drain region 14. The well 12 extends down underneath the drain diffusion 14 and laterally underneath the field oxide areas 13. In the exemplary embodiment, the edge areas of the p well 12 are made to extend under the gate electrode 18 which is insulated from the two wells 11 and 12 and source 15 by means of the gate oxide 17.

On page 7, amend the paragraph beginning on line 24 as follows:

The gate electrode 18 is embodied, for example, as a polysilicon layer and extends from the ~~gate 18 as far as~~ source 15 toward and over the field oxide 13 in the direction of the drain 14. If this highly conductive, lengthened gate electrode is arranged above the well 12, it serves as a field plate for controlling the electric field in the edge area of the well 12. At a higher level, the metal 1 level in the exemplary embodiment, a metal layer 19 is provided above the polysilicon field plate, said metal layer 19 extending further in the direction of the drain 14 between the gate 18 and drain 14 above the field oxide 13. The metal layer 19 is electrically connected to the gate electrode 18 by means of a via 20.

On page 8, amend the paragraph beginning on line 1 as follows:

Figure 1 illustrates a flat p-doped well 21 underneath the drain region, said well 21 being per se unnecessary but being advantageously produced in transistors for particularly high voltages. The flat p-doped well ~~17~~ 21 is typically embodied as a retrograde well with boron and an energy of less than 150 kV as well as a concentration of approximately 10^{13} [[cm^{-3}]] cm^{-2}. A short drive-in step is carried out. The p-doped well area 21 ends 0.5 µm under the silicon surface. This well brings about a concentration in its well region which is lower than the drain doping and higher than the doping with the p-doped well 12. The doping therefore decreases uniformly from the drain diffusion in the direction of the substrate, as a result of which excessive increases in the electrical field strength or a breakdown are avoided.

On page 9, amend the paragraph beginning on line 29 as follows:

It has become apparent that with a high-voltage PMOS transistor according to Figure 1, on the one hand the dielectric strength is increased owing to the large distance between the points A' and C', and on the other hand the distance A'-B' is sufficiently large to prevent a punch through from the p-doped well 12 to the substrate 10.

On page 10, amend the paragraph beginning on line 9 as follows:

A mask Mn, which is outlined in a basic form above the transistor in Figure 1, is manufactured on the undoped wafer as a first step. In the process, the mask is applied in such a way that areas ~~21~~ 26 and 22 through which no implantation of ions is possible are produced. Then, an ion implantation In in which phosphorous ions are implanted with an energy of 300 kV and a dose of preferably 8.3 x 10^{12} [[cm^{-3}]] cm^{-2} is carried out through the window Wn and the

areas lying outside the mask part 22. Phosphorous ions which are more mobile than, for example, arsenic ions, are preferably implanted during the thermal diffusing-out process so that, with the exception of the shaded areas ~~21~~ 26 and 22, a relatively uniform distribution of the doping of phosphorous is produced in the well 11.

On page 10, amend the paragraph beginning on line 25 as follows:

The mask which is used here is illustrated in the basic form with reference to Figure 2. The masking ~~21~~ 26 covers the central area of the drain. A further cover 22, which lies between the areas of the drain zone which is provided and the source diffusion which is provided, is provided at a distance from the drain cover 21. In the exemplary embodiment of Figure 2, this further cover is embodied in a strip shape. The mask Mn which is outlined in Figure 1 is illustrated as a cross section along the line 1A and 1B through the mask in Figure 2.

On page 12, amend the paragraph beginning on line 10 as follows:

Implantation Ip with p ions, for example boron ions, is subsequently carried out through the exposed areas Wp which are not covered by the masking. This implantation is carried out in two steps, once with, for example, an energy of 300 kV and a dose of 5×10^{12} [[cm^{-3}]] cm^{-2}, and in the second step with an energy of, for example, 150 kV and also a dose of 5×10^{12} [[cm^{-3}]] cm^{-2}. Of course, both the energy and the dose can be changed depending on the type of manufacturing process used. The stated doses relate here to a process using technology with a structure width of 0.35 µm.

On page 13, after line 20, insert the following paragraph:

The scope of protection of the invention is not limited to the examples given hereinabove. The invention is embodied in each novel characteristic and each combination of characteristics, which includes every combination of any features which are stated in the claims, even if this combination of features is not explicitly stated in the claims.